Remarks

Claims 1-13 and 22-25 are pending in the present application. Reconsideration and allowance are requested in view of the above amendments and the remarks below. Applicants do not acquiesce in the correctness of the rejections and reserve the right to present specific arguments regarding any rejected claims not specifically addressed. Furthermore, Applicants reserve the right to pursue the full scope of the subject matter of the original claims in a subsequent patent application that claims priority to the instant application.

Claims 1, 2, 5, 15, 16, 19, and 21 are rejected under 35 U.S.C. 103(a) over Fan (U.S. 2004/0047361) in view of Madany (U.S. 6,938,134). Claims 1, 3, 4, 15, 17, 18, and 22 are rejected under 35 U.S.C. 103(a) over Cornet (U.S. 2003/0137936) in view of Madany. Claim 14 is rejected under 35 U.S.C. 103(a) over Fan and Madany in view of Arimoto (5,798,976). These rejections are defective because Fan, Madany, and Cornet, taken alone or in any combination, fail to disclose each and every feature of the claims as required by 35 U.S.C. 103(a).

Claim 1 sets forth:

> "A method for dynamically managing a reassembly buffer, comprising:
> providing a plurality of data blocks and an indirect list;
> pointing, via entries in the indirect list, to allocated data blocks in the plurality of data blocks that currently store incoming data;
> if a free data block in the plurality of data blocks is required for the storage of incoming data, allocating the free data block for storing incoming data; and,
> if an allocated data block in the plurality of data blocks is no longer needed for storing incoming data, deallocating the allocated data block such that the deallocated data block becomes a free data block; and selectively operating the reassembly buffer in a static mode by not deallocating allocated data blocks."

As admitted by the Examiner, Fan and Madany are "silent on selectively operating the reassembly buffer in a static mode by not deallocating data blocks." Applicants agree. To remedy the glaring deficiencies of Fan and Madany, the Examiner relies on the disclosure of Arimoto. In particular, the Examiner has incorrectly equated Arimoto's address buffer with the claimed "reassembly buffer" and has incorrectly interpreted the operation of Arimoto's address buffer by stating that Arimoto operates the address buffer in a static mode "by not deallocating data blocks."

First, contrary to the assertions of the Examiner, Arimoto's address buffer is not equivalent to the claimed "reassembly buffer." The claimed "reassembly buffer" and Arimoto's address buffer operate in different manners and for different purposes. Further, the static mode of Arimoto's address buffer is not accomplished by "not deallocating data blocks." Rather, Arimoto discloses (see, col. 23, lines 1-9) that in "the data holding mode operation, data holding mode designation signal REF is at H-level. In this state, the output signals of OR circuit 62a and 62b are held at H-level. In row address buffer circuit 16a, therefore, transfer gate 16aa maintains the on state, and NAND circuits 16ae and 16ad function as inverters. Thus, row address buffer circuit 16a operates statically to produce signal bits RA and /RA which change in accordance with the signal bits applied from multiplexer 14." Thus, the static mode of Arimoto's address buffer refers to the production of signal bits RA and /RA, and not is not associated with the deallocation or lack thereof of data blocks.

A large number of claims, namely claims 6-13, 20, and 23-25, were improperly rejected by the Examiner, **without any supporting evidence**, as being neither novel nor patentable for allegedly comprising known engineering techniques and producing

predictable results. Applicants strenuously disagree with the Examiner's position and request that the Examiner provide a thorough examination of all of the claims as entitled by Applicants. Applicants submit that claims 6-13, 20 set forth specific novel and patentable details regarding the structure and operation of the claimed "free list," while claims 23 and 24-25 set forth specific novel and patentable details regarding the claimed "indirect list" and "sequence number," respectively.

Accordingly, Applicants submit that independent claim 1 and its corresponding dependent claims are allowable. Applicants further submit that independent claim 22 and its corresponding dependent claims are allowable for reasons similar to those set forth above with regard to independent claim 1.

With respect to the dependent claims, Applicants herein incorporate the arguments presented above with respect to the independent claims from which the claims depend. The dependent claims are believed to be allowable based on the above arguments, as well as for their own additional features.

Applicants submit that each of the pending claims is patentable for one or more additional unique features. To this extent, Applicants do not acquiesce to the Examiner's interpretation of the claimed subject matter or the references used in rejecting the claimed subject matter. Additionally, Applicants do not acquiesce to the Examiner's analysis, combinations, and modifications of the various references or the motives cited for such combinations and modifications. These features and the appropriateness of the Examiner's combinations and modifications have not been separately addressed herein for brevity. However, Applicants reserve the right to present such arguments in a later response should one be necessary.

If the Examiner believes that anything further is necessary to place the application in condition for allowance, the Examiner is requested to contact Applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,

/ John A. Merecki /

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